



PXle-5413

User Manual



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PXIe-5413

PXIe, 20 MHz Bandwidth, 16-Bit PXI Waveform Generator

- 200 MS/s sampling rate
- 0.00775 V_{pk-pk} to 12 V_{pk-pk} output amplitude into a 50 Ω load
- 0 MHz to 20 MHz sine wave generation
- 0 MHz to 10 MHz square wave generation
- 0 MHz to 1 MHz ramp and triangle wave generation
- Standard function, arbitrary waveform, arbitrary sequence, and frequency list output modes
- Single, continuous, stepped, and burst trigger modes when configured to frequency list, arbitrary waveform, or arbitrary sequence output modes
- Independent channels (two-channel PXIe-5413 only)
- NI-TClk synchronization

Related information:

- [NI-TClk Manual](#)

PXIe-5413 Pinout and LEDs

Front Panel

Refer to the following figure and tables for information about the one- and two-channel PXIe-5413 front panel connectors and LEDs.

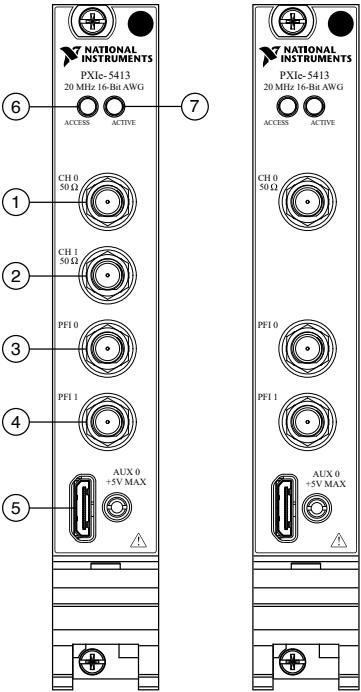


Table 1. PXIe-5413 Signal Descriptions

	Signal	Connector Type	Access	Description
1	CH 0	SMA	Output	Generates waveforms from an analog output terminal.
2	CH 1			
3	PFI 0		Input/Output	Imports digital trigger signals and exports digital event signals. Imported digital trigger signals can start or step through waveform generation, and exported event signals indicate the state of the generation engine.
4	PFI 1			
5	AUX 0	MHDMR		Routes digital trigger and event signals with eight bidirectional PFI lines and provides a +3.3 V power source.

Table 2. PXIe-5413 ACCESS LED IndicatorsThe ACCESS LED indicates basic hardware status.

	LED Color	Indication
6	No color (off)	The PXIe-5413 is not yet functional.
	Amber	The PXIe-5413 is being accessed.
	Green	The PXIe-5413 is ready to be programmed by NI-FGEN.

Table 3. PXle-5413 ACTIVE LED IndicatorsThe ACTIVE LED indicates the PXle-5413 hardware state.

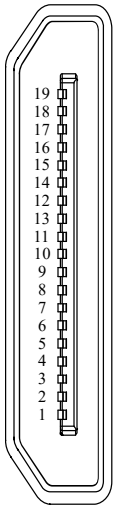
	LED Color	Indication
7	No color (off)	The PXle-5413 is not generating.
	Amber	The PXle-5413 is armed and waiting for a trigger.
	Green	The PXle-5413 has received a trigger and is generating a waveform.
	Red	The PXle-5413 has detected an error. NI-FGEN must access the PXle-5413 to determine the cause of the error. The LED remains red until the error condition is removed. Example errors include the following: - Phase-locked loop (PLL) unlocked: The PXle-5413 has detected an unlocked condition on a previously locked PLL. A PLL that is unlocked while in reset does not show an error. - The PXle-5413 has powered down because the internal temperature exceeded the maximum limit. The over-temperature condition must be corrected and the hardware reset. To reset the hardware, call niFgen Reset Device or niFgen_ResetDevice.^[1]

Connector



Note The AUX 0 connector accepts a standard, third-party HDMI™ type C cable, but the AUX 0 port is not an HDMI interface and the specified performance of the AUX 0 connector is not guaranteed if a third-party HDMI cable is used. Use NI cable assembly SHH19-MH19-AUX for all AUX 0 connections. Do not connect the AUX 0 port on the PXle-5413 to the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.

Refer to the following figure and table for information about the PXle-5413AUX 0 connector pins.

**Table 4.** AUX 0 Pin Signal Descriptions

Pin	Signal	Description
1	GND	Ground reference for signals
2	NC	No connection
3	GND	Ground reference for signals
4	GND	Ground reference for signals
5	NC	No connection
6	GND	Ground reference for signals
7	GND	Ground reference for signals
8	AUX 0/PFI 0	Bidirectional PFI line
9	AUX 0/PFI 1	Bidirectional PFI line
10	GND	Ground reference for signals
11	AUX 0/PFI 2	Bidirectional PFI line
12	AUX 0/PFI 3	Bidirectional PFI line
13	GND	Ground reference for signals
14	AUX 0/PFI 4	Bidirectional PFI line
15	AUX 0/PFI 5	Bidirectional PFI line
16	AUX 0/PFI 6	Bidirectional PFI line
17	AUX 0/PFI 7	Bidirectional PFI line
18	+3.3 V	+3.3 V power output (200 mA maximum)

Pin	Signal	Description
19	GND	Ground reference for signals

Related reference:

- [PXIe-5413 SCB-19 Pinout](#)

PXIe-5413 SCB-19 Pinout

NI recommends using the SCB-19 connector block to connect digital signals to the AUX 0 connector on the PXIe-5413 front panel. Refer to the following figure and table for information about the SCB-19 signals when connected to the AUX 0 front panel connector.

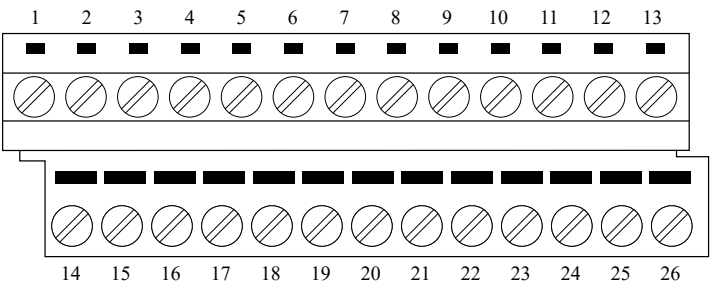


Table 5. SCB-19 Signal Descriptions

Pin	Signal	Description
1	PFI 0	Bidirectional PFI line
2	PFI 1	Bidirectional PFI line
3	PFI 2	Bidirectional PFI line
4	PFI 3	Bidirectional PFI line
5	NC	No connection
6	NC	No connection
7	NC	No connection
8	NC	No connection
9	PFI 4	Bidirectional PFI line
10	PFI 5	Bidirectional PFI line

Pin	Signal	Description
11	PFI 6	Bidirectional PFI line
12	PFI 7	Bidirectional PFI line
13	+3.3 V	+3.3 V power (200 mA maximum)
<14..26>	GND	Ground reference for signals

Related reference:

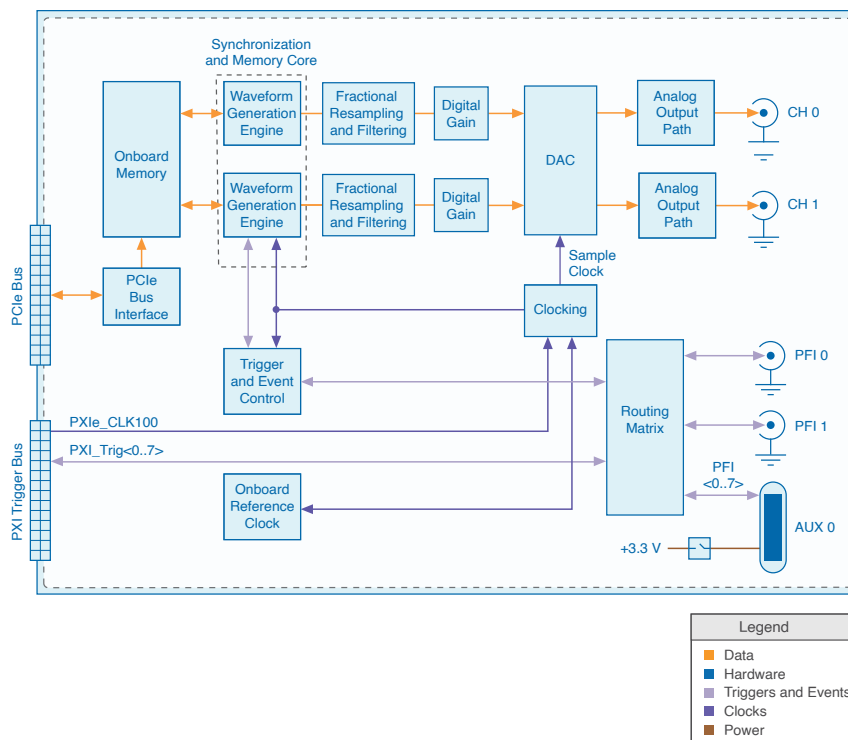
- [PXle-5413 Pinout and LEDs](#)

Related information:

- [PXle-54x3 Pinout and LEDs](#)

PXle-5413 Block Diagram

The PXle-5413 generates analog output signals from digital waveform data at the CH connectors and routes trigger, event, and clock signals.



- **Onboard Memory**—Stores the waveform data and generation instructions that you load into the PXIe-5413.
- **Waveform Generation Engine**—Retrieves the waveform data and instructions from the onboard memory and triggers from Trigger and Event Control using the Sample Clock.
- **Fractional Resampling and Filtering**—Resamples (digital signal processing) and filters images.
- **Digital Gain**—Applies digital gain to the signal.
- **DAC**—Converts 16-bit digital waveform data.
- **Analog Output Path**—Filters, amplifies, and attenuates the waveform data retrieved from the DAC.
- **Clocking**—Creates and distributes the Sample Clock.
- **Onboard Reference Clock**—Provides the default Reference Clock source.
- **Trigger and Event Control**—Sends triggers and events to the Waveform Generation Engine and Routing Matrix.
- **Routing Matrix**—Routes triggers and events between PXI trigger lines and PFI terminals.

Related concepts:

- [PXIe-5413 Analog Output Path](#)
- [PXIe-5413 Fractional Resampling and Filtering](#)

- [PXIe-5413 Clocks](#)

Related reference:

- [PXIe-5413 Routes](#)

PXIe-5413 Routes

The following table summarizes routes that can be created with the PXIe-5413.

Source	Destination			
	PXI_Trig Terminals	PFI Terminals	Triggers	Sync Pulse
PXI_Trig Terminals	—	—	✓	✓
PFI Terminals	—	—	✓	—
Events	✓	✓	✓	—
Triggers	✓	✓	✓	—
Sync Pulse	✓	—	—	—

The following table lists all possible values for PXIe-5413 sources and destinations.

PXI_Trig Terminals	PFI Terminals	Events ^[1]	Triggers ^[1]	Sync Pulse
PXI_Trig0	PFI0	0/ReadyForStartEvent	0/StartTrigger	Clock10Pulse
PXI_Trig1	PFI1	0/StartedEvent	0/ScriptTrigger0	
PXI_Trig2	AUX0/PFI0	0/DoneEvent	0/ScriptTrigger1	
PXI_Trig3	AUX0/PFI1	0/Marker0Event	0/ScriptTrigger2	
PXI_Trig4	AUX0/PFI2	0/Marker1Event	0/ScriptTrigger3	

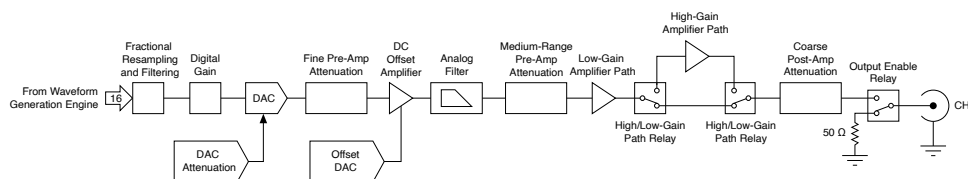
PXI_Trig Terminals	PFI Terminals	Events ^[1]	Triggers ^[1]	Sync Pulse
		0/Marker2Event		
		0/Marker3Event		
	AUX0/PFI3	1/ReadyForStartEvent	1/StartTrigger	
PXI_Trig5	AUX0/PFI4	1/StartedEvent	1/ScriptTrigger0	
PXI_Trig6	AUX0/PFI5	1/DoneEvent	1/ScriptTrigger1	
PXI_Trig7	AUX0/PFI6	1/Marker0Event	1/ScriptTrigger2	
	AUX0/PFI7	1/Marker1Event	1/ScriptTrigger3	
		1/Marker2Event		
		1/Marker3Event		

Related information:

- [NI-TClk Manual](#)

PXIe-5413 Analog Output Path

The two-channel PXIe-5413 supports independent-channel waveform generation.



The following processes outline the generation of analog waveforms with the PXIe-5413:

1. The 16-bit digital waveform data from the Waveform Generation Engine is passed through fractional resampling and filtering.



Note When the PXle-5413 is configured to standard function output mode, the signal bypasses fractional resampling and filtering.

You can enable or disable digital filtering using niFgen Configure Digital Filter, niFgen_EnableDigitalFilter, or niFgen_DisableDigitalFilter. By default, the digital filter is enabled.

2. The signal passes through a digital gain circuit.

Digital gain multiplies waveform data by a factor you specify with the Digital Gain property or the NIFGEN_ATTR_DIGITAL_GAIN attribute before converting the data to an analog signal in the DAC.

Digital gain can be changed during waveform generation without the glitches caused by switching that are common when changing analog gain. However, the output resolution of the DAC is a function of digital gain, meaning that only analog gain makes full use of the resolution of the DAC.

3. The signal passes through the 800 MS/s DAC.
4. The signal passes through fine preamplifier attenuation: a set of selectable solid-state attenuators that provide 0 dB to 2.4 dB of signal attenuation in sixteen 0.16 dB increments. The final 0.16 dB increment uses DAC-code scaling to configure the exact amplitude based on the gain setting.
5. The signal passes through a DC offset amplifier that adds the specified DC offset voltage.

You can adjust the amount of DC offset added to the signal, up to one-half of the value of the gain setting, by using either the Arbitrary Waveform Offset property or DC Offset property, or the NIFGEN_ATTR_ARB_OFFSET or NIFGEN_ATTR_FUNC_DC_OFFSET attributes.

6. The signal passes through an enabled 20 MHz time-domain, Bessel analog filter. The enabled analog filter increases the delay from the time at which the PXle-5413 receives a trigger to the time at which the analog output signal is generated.



Note When the PXle-5413 is configured for sine wave generation in standard function output mode, the signal bypasses the time-domain,

Bessel filter.

7. The signal passes through medium-range preamplifier attenuation: a set of selectable solid-state attenuators that provide 0 dB to 10.23 dB of attenuation in five 2.56 dB increments.

You can adjust the amount of attenuation by configuring the Arbitrary Waveform Gain property or Amplitude property, or the NIFGEN_ATTR_ARB_GAIN or NIFGEN_ATTR_FUNC_AMPLITUDE attributes. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.

8. The signal continues through either the low-gain amplifier path or high-gain amplifier path.
 - The low-gain amplifier path is used for waveforms that have all output voltages equal to or less than ± 2.75 V into 50 Ω loads. The low-gain amplifier has a fixed gain.
 - The high-gain amplifier path is used for waveform output voltages greater than ± 2.75 V into 50 Ω loads. The high-gain amplifier has a fixed gain and enables maximum peak-to-peak signal amplitude (V_{pk-pk}).

By default, NI-FGEN automatically selects the amplifier path the signal passes through based on the gain or amplitude setting.

	Maximum Gain ($V_{pk-center}$)	Maximum Amplitude (V_{pk-pk})
50 Ω load impedance	6	12
1 M Ω load impedance	12	24

Alternatively, you can use the Analog Path property or the NIFGEN_ATTR_ANALOG_PATH attribute to set the signal path to remain constant regardless of the gain setting for applications requiring only one of the amplifier paths. Configuring a constant signal path through the low-gain amplifier path regardless of the gain setting affects the maximum output value allowable for that particular gain setting: The maximum gain setting for signals configured to use the low-gain amplifier path is 2.75.

9. The signal passes through coarse postamplifier attenuation: a set of two passive attenuators that provide 0 dB to 38.37 dB of attenuation in four 12.79 dB increments.

You can adjust the amount of attenuation by configuring either the Arbitrary Waveform Gain property or Amplitude property, or the NIFGEN_ATTR_ARB_GAIN attribute or NIFGEN_ATTR_FUNC_AMPLITUDE attribute. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain or amplitude settings.

At this point, the signal has an applied maximum attenuation of 51 dB. After this point, the signal will continue to digitally attenuate.

10. The signal passes through the output enable relay.
 - When the relay is disabled, ground is connected to the output through a 50 Ω resistor. Waveform generation continues while the output enable relay is disabled.
 - When the relay is enabled, the analog waveform is generated at the analog output connector.

You can enable or disable analog output using niFgen Output Enable or niFgen_ConfigureOutputEnabled.



Note When you change a setting that results in a relay switch, the bouncing of electromechanical relays on the PXle-5413 distorts the output signal for about 10 ms.

Related concepts:

- [PXle-5413 Fractional Resampling and Filtering](#)

PXle-5413 Fractional Resampling and Filtering

The 16-bit digital waveform data from the Waveform Generation Engine can pass through two resampling digital signal processing (DSP) paths: digital filter enabled or digital filter disabled.

You can select the path for the signal to pass through by enabling or disabling the digital filter using `niFgen Configure Digital Filter`, `niFgen_EnableDigitalFilter`, or `niFgen_DisableDigitalFilter`. By default, the digital filter is enabled.

When the PXIe-5413 is configured to standard function output mode, the signal bypasses fractional resampling and filtering.

Digital Filter Disabled

With the digital filter disabled, the waveform output includes an update step at the sample rate you specify with `niFgen Set Sample Rate` or the Sample Rate property. As a result, the waveform output includes images of the original waveform at multiples of the sample rate.

Analog filtering later in the signal path causes the images to roll-off beyond 20 MHz.

The following figures show 2.5 MHz sine waveform generation at 50 MS/s with the digital filter disabled.

Figure 1. Time Domain

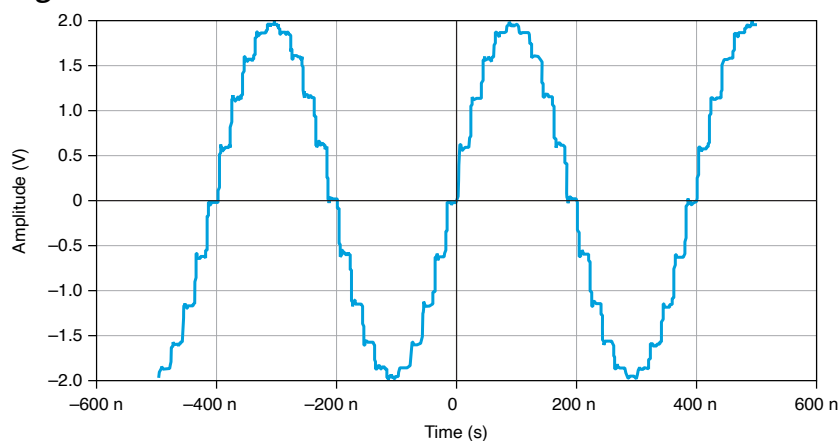
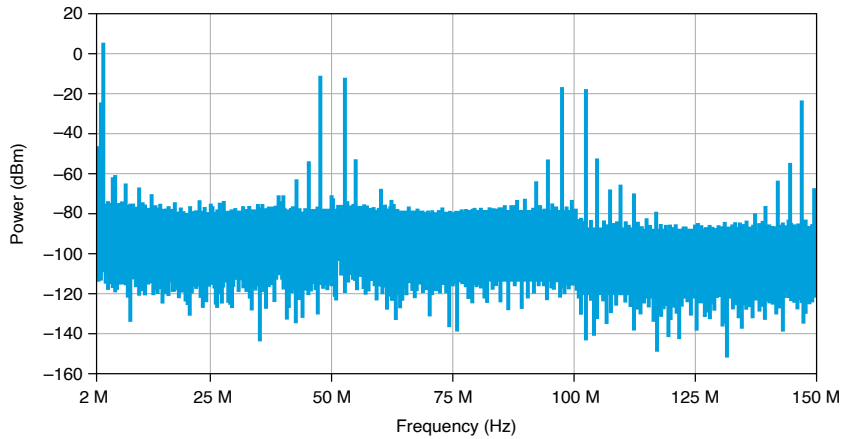


Figure 2. Power Spectrum

Digital Filter Enabled

With the digital filter enabled, images at multiples of the sample rate are removed from the waveform output.

The following figures show 2.5 MHz sine waveform generation at 50 MS/s with the digital filter enabled.

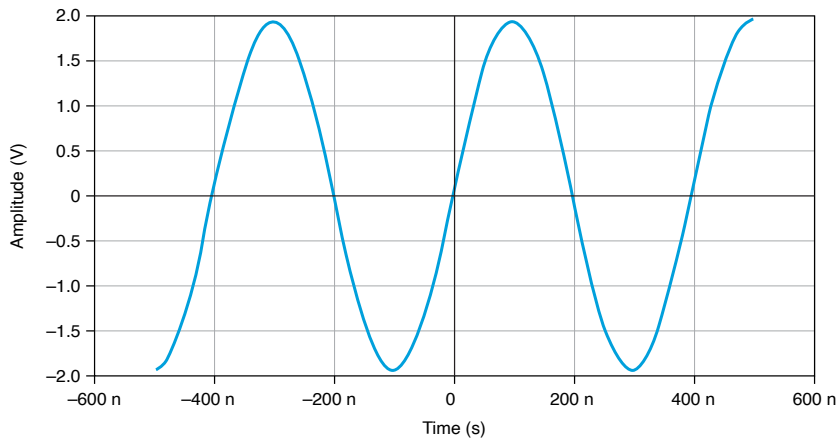
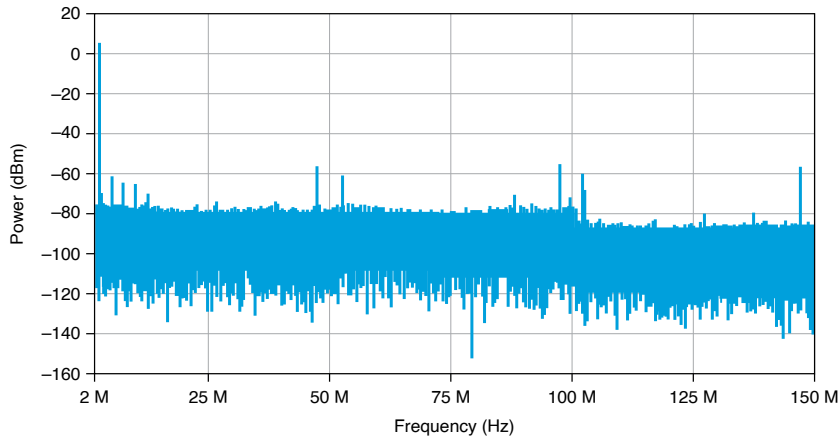
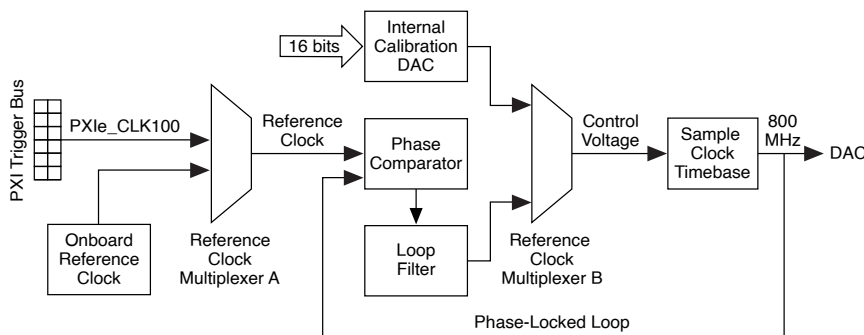
Figure 3. Time Domain

Figure 4. Power Spectrum**Related concepts:**

- [PXIe-5413 Analog Output Path](#)

PXIe-5413 Clocks



Sample Clock (Internal)

The Sample Clock signals when the DAC converts the digital waveform values to an analog voltage. The PXIe-5413 can derive a Sample Clock from its main internal timing source, the onboard Sample Clock Timebase. The PXIe-5413 uses a high-precision 100 MHz voltage-controlled crystal oscillator (VCXO) clock source for the Sample Clock Timebase.

The Sample Clock Timebase frequency is tuned by an internal calibration DAC control voltage when the Reference Clock Source property or the NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE attribute is set to **None**. The internal calibration DAC, which is calibrated at the factory and which you also can calibrate, tunes the Sample Clock Timebase to maintain a high quality frequency source.

The PXIe-5413 only supports **High-Resolution** clock mode and does not support external Sample Clock sources.

Reference Clock

The PXIe-5413 uses either the onboard Reference Clock, a temperature-compensated crystal oscillator (TCXO), or the PXIe_CLK100 backplane line as the Reference Clock source. The source provides the control voltage that tunes the VCXO of the Sample Clock Timebase to match the frequency stability and accuracy of the Reference Clock source for internal clock update sources, using a phase-locked loop (PLL).

To begin the PLL, the phase comparator compares the selected Reference Clock to the 100 MHz clock of the Sample Clock Timebase. Next, a control voltage proportional to the phase difference between the two clocks is developed and used to tune the Sample Clock Timebase into alignment with the Reference Clock. Finally, the Sample Clock Timebase output is routed back to the phase comparator, and the loop is closed.

You can synchronize the PXIe-5413 with other instruments using `PXIe_Clk100` as the Reference Clock source and NI-TClk.

Related concepts:

- [PXIe-5413 Synchronization](#)

Related information:

- [NI-TClk Manual](#)

PXIe-5413 Synchronization

The PXIe-5413 supports synchronization using the NI-TClk API with a single NI-FGEN session per PXIe-5413. NI-TClk synchronization support for the PXIe-5413 was first available in NI-FGEN18.1.

You can synchronize the PXIe-5413 with other instruments using `PXIe_Clk100` as the Reference Clock source and NI-TClk.

Use the NI-FGENAbsolute Delay property or NIFGEN_ATTR_ABSOLUTE_DELAY attribute to reduce trigger jitter or to maintain synchronization repeatability when synchronizing multiple instruments with NI-TClk. Phase DAC adjustment is not supported.

Synchronization with a Two-Channel

The channels of a two-channel PXIe-5413 are automatically synchronized when they are in the same NI-FGEN session.

Synchronization with NI-TClk is not supported with multiple channel-based NI-FGEN sessions to a single two-channel PXIe-5413.

Related information:

- [NI-TClk Manual](#)

PXIe-5413 Power On and Device Reset

The PXIe-5413 has different settings when powering on and after powered on or a device reset.

The PXIe-5413 is in the following state from the time at which the computer begins to power on until the operating system has started and NI-FGEN is loaded.

CH <0..1>	PFI <0..1>	PXI_Trig <0..7>
• Analog output is disabled. • 0 V amplitude • 50 Ω output impedance to ground	• Tristated	• Tristated and floating

When the operating system has started and NI-FGEN is loaded or after performing a device reset, the PXIe-5413 is in the following state.

CH <0..1>	PFI <0..1>	PXI_Trig <0..7>	Clocks
• Analog output is enabled. • 0 V amplitude • 0 dB attenuation • Low-gain amplifier path is enabled.	• Tristated	• Tristated and floating	• Sample Clock Timebase is set to use the internal voltage-controlled crystal oscillator (VCXO).