



PXle-5171

User Manual



Provided by:

Test & Measurement Automation

Embedded Control & Monitoring

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PXIe-5170/5171

This section includes useful information about the PXIe-5170/5171 reconfigurable oscilloscopes, including front panel connectors, theory of operation, signal path information, block diagrams, and calibration information.



Note NI provides two software options for programming the PXIe-5170/5171: NI-SCOPE instrument driver software and LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes. Refer to the PXIe-5170/5171 Getting Started Guide for more information about choosing the right software for your application.

The PXIe-5170/5171 includes the following features:

- Up to 8 channels
- 14-bit resolution with 5 voltage ranges
- 250 MS/s sample rate with internal or external clocking support
- Up to 250 MHz bandwidth (PXIe-5171)
- User-programmable with LabVIEW FPGA Module
- Gen 2 x8 PXI Express
- NI-TClk synchronization using the NI-SCOPE API

Looking for Something Else?

For information not found in the User Manual for your product, such as specifications and API reference, browse ***Related Information***.

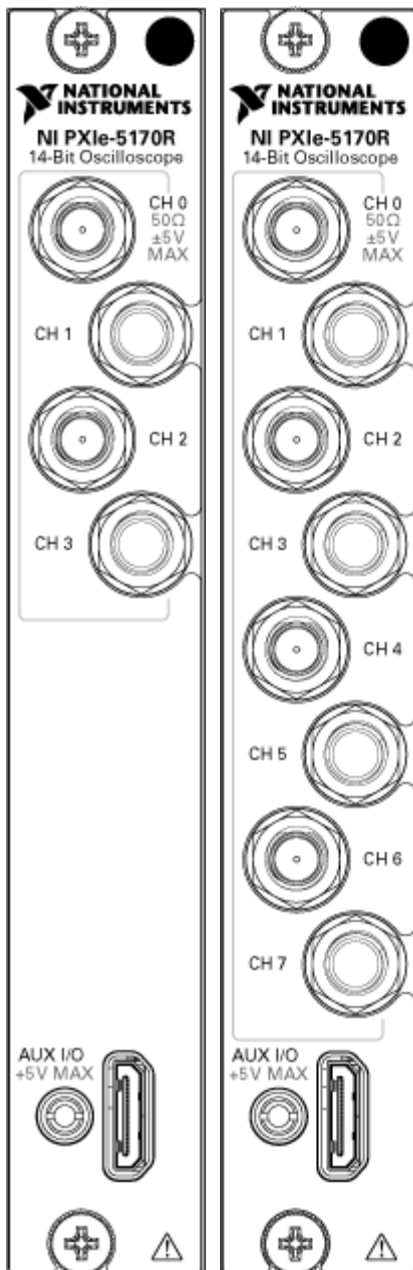
Related information:

- [PXIe-5170 Specifications](#)
- [PXIe-5171 Specifications](#)
- [NI-SCOPE User Manual](#)
- [Software and Driver Downloads](#)
- [Release Notes](#)
- [License Setup and Activation](#)

- [Dimensional Drawings](#)
- [Product Certifications](#)
- [Letter of Volatility](#)
- [Discussion Forums](#)
- [NI Learning Center](#)

Front Panels

This section describes the front panel and connectors of the 4 CH and 8 CH variants of the .



Front Panel Connectors

Label	Connector Type	Function
CH 0—CH 3	SMA connector	Analog input terminal
CH 4—CH 7	SMA connector	Additional analog input terminals on the (8 CH)

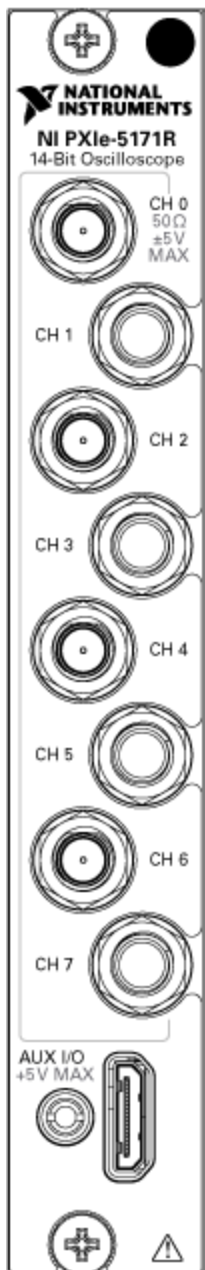
Label	Connector Type	Function
AUX I/O	MHDMR connector	Sample Clock or Reference Clock input, Reference Clock output, bidirectional digital PFI, and 3.3 V power output  Note This connector is referred to as AUX 0 in this document.



Note The AUX 0 connector accepts a standard, third-party HDMI™ type C cable, but the AUX 0 port is not an HDMI interface and the specified performance of the AUX 0 connector is not guaranteed if a third-party HDMI cable is used. Use NI cable type SHH19-MH19-AUX for all AUX 0 connections. Do not connect the AUX 0 port on the to the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.

Front Panel

This section describes the front panel and connectors of the .



Front Panel Connectors

Label	Connector Type	Function
CH 0—CH 7	SMA connector	Analog input terminal
AUX I/O	MHDMMR connector	Sample Clock or Reference Clock input, Reference Clock output, bidirectional digital PFI, and 3.3 V power output

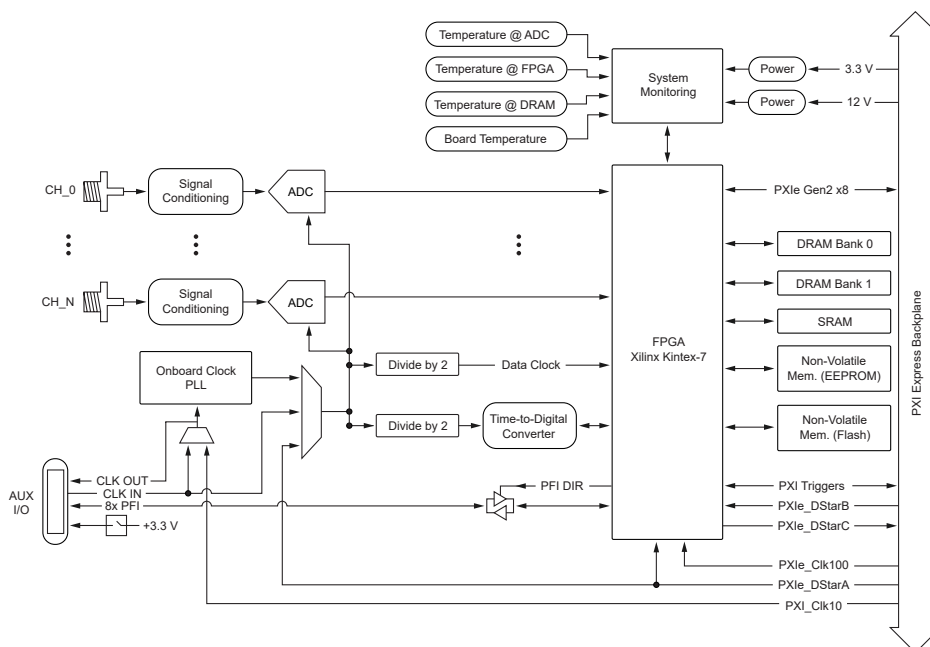
Label	Connector Type	Function
		 Note This connector is referred to as AUX 0 in this document.



Note The AUX 0 connector accepts a standard, third-party HDMI™ type C cable, but the AUX 0 port is not an HDMI interface and the specified performance of the AUX 0 connector is not guaranteed if a third-party HDMI cable is used. Use NI cable type SHH19-MH19-AUX for all AUX 0 connections. Do not connect the AUX 0 port on the to the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.

Block Diagram

The PXle-5170 and PXle-5171 are represented by the following high-level block diagram. Channel count has been abstracted.



The PXle-5170/5171 has the following subsystems:

Signal Conditioning

Clocking

PFI

PXI Trigger Resources

External Power

DRAM

PXIe-5170/5171 System Monitoring and Shutdown

The PXIe-5170/5171 has onboard power and temperature monitoring. You can access these measurements through the instrument design libraries and FPGA I/O. These measurements are used as protection limits to prevent device damage in the case of excessive power or temperature across the device.

Related concepts:

- [FPGA I/O Elements](#)

Thermal Monitoring and Shutdown

The PXIe-5170/5171 is protected against excessive temperatures and shuts down in the presence of excessive heat. In the event of an over temperature condition, the system responds at two set points. At an initial limit, the hardware and software will generate an error signal in the FPGA warning the user of a fault condition. Should the fault not be cleared and the temperature reaches a critical limit that may result in device damage, the device will shut itself down.

(NI-SCOPE) If the device powers down, you are notified with an error message in one of the following ways:

- NI-SCOPE returns an error when you use any of the functions that program the hardware or check hardware status, such as the commit function and the self-calibration function.
- MAX returns an error message if you run a self-test on your device after it exceeds

the thermal shutdown temperature.

Re-enabling the Device After Thermal Shutdown

To re-enable your device after thermal shutdown, use one of the following methods:

- Power down the computer connected to the device.
- Disable and enable the device from the Device Manager.

During normal operation, the thermal protection should not engage over the rated ambient temperature range of the device, provided that the power consumption remains below 100% of the allowed power.

You can read the device temperature using the instrument design libraries. Refer to Configuration Overview for more information.

Power Monitoring and Shutdown

To stay within PXI Express power and cooling requirements, there may be limitations on the size and activity factor of the logic loaded to the FPGA. You can access onboard power sensors to evaluate the power draw of a particular design, allowing you to balance design capabilities with power limitations.

Should power consumed by the device exceed a factory-programmed limit, the device will generate a signal on an FPGA I/O Node that indicates an over-power condition and shut itself down.

(NI-SCOPE) In the event that the device powers down, you are notified with an error message in one of the following ways:

- NI-SCOPE returns an error when you use any of the functions that program the hardware or check hardware status, such as the commit function and the self-calibration function.
- MAX returns an error message if you run a self-test on your device after it exceeds the power shutdown limit.

Re-enabling the Device After Power Shutdown

To re-enable your device after power shutdown, use one of the following methods:

- Power down the computer connected to the device.
- Disable and enable the device from the Device Manager.

Power Planning

If your device is installed in a chassis and slot that allows for more power than the minimum required by the PXI Express specification, it is possible to operate your device with higher power, as long as the device does not exceed its thermal limits. This allows you to increase performance if your device is operating in a cool environment. Refer to your chassis documentation to understand how much system and slot power it provides to peripheral modules.

Signal Conditioning

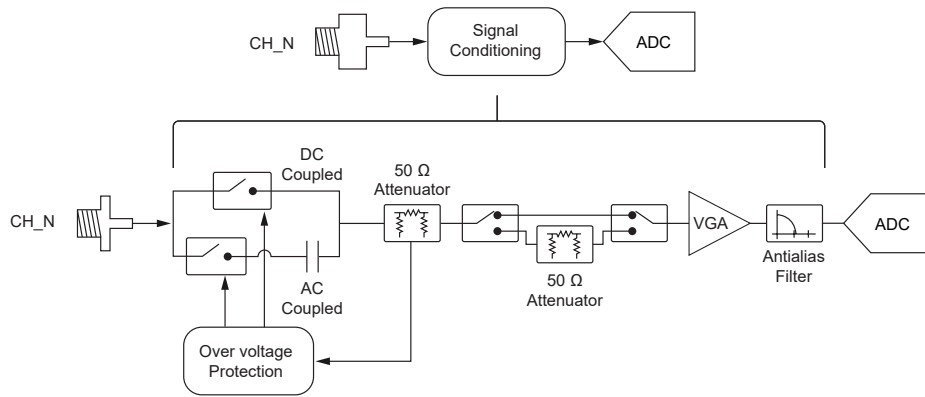
The PXIe-5170/5171 provides users with a range of front end configurations, including selectable ranges, coupling, and filtering.



Note A variable gain amplifier (VGA) is used in both devices to provide multiple voltage ranges.

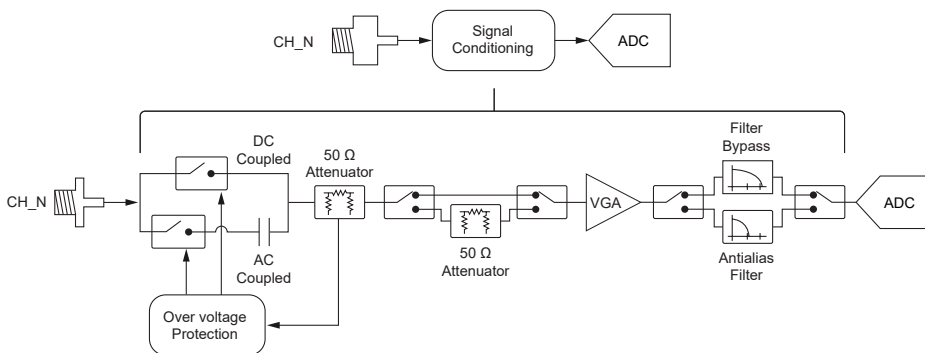
PXIe-5170 Block Diagram

The PXIe-5170 has 4 or 8 channels whose individual high-level functions are represented below.



PXIe-5171 Block Diagram

The PXIe-5171 has 8 channels whose individual high-level functions are represented below.



PXIe-5170/5171 Input Coupling

You can select AC or DC input coupling with 50 Ω input impedance. AC coupling allows you to reject the DC components of a signal. For information about the AC coupling cutoff frequency or AC flatness, refer to the device specifications.

Related information:

- [Input Coupling](#)
- [PXIe-5170 Specifications](#)
- [PXIe-5171 Specifications](#)

PXle-5170/5171 Input Ranges

The PXle-5170/5171 allows the following software-selectable input voltage ranges (V_{pk-pk}): 0.2 V, 0.4 V, 1 V, 2 V, and 5 V. These ranges are ground referenced, and do not have programmable offset control. Signals exceeding these ranges will be affected by the protection circuitry.

Related concepts:

- [PXle-5170/5171 Protection](#)

PXle-5170/5171 Protection

The PXle-5170/5171 channels are protected for transient and overvoltage conditions. If a signal exceeds the absolute maximum rating of ± 5 V, the protection circuitry will attempt to clamp the signal to a safe voltage level.

If the signal exceeds the input range to the point where damage may occur, the protection circuit will open the two front end relays, disconnecting the signal from the oscilloscope electronics. This event generates a signal to the FPGA which you can monitor for error conditions. After opening, the front end switches will close again every 200 ms. If the overvoltage condition is still present, the switches will re-open. This cycle will continue until the condition is cleared, at which point the switches will close and remain closed.

PXle-5170/5171 Anti-Alias Filter

The PXle-5170/5171 has an anti-alias filter path for capturing signals in the first Nyquist zone. This filter is a 100 MHz cutoff filter whose primary purpose is to reject signals that may otherwise alias into the spectrum of the 250 MS/s ADC. For information about the AC flatness of this filter, refer to the device specifications.

The PXle-5171 allows you to bypass the anti-alias filter to capture higher-frequency, band-limited signals.

Related information:

- [PXIe-5170 Specifications](#)
- [PXIe-5171 Specifications](#)

PXI Ground Loop Noise

Some electronic systems can induce ground loop noise in measurements taken with instruments with multiple ground connections. Spurious DC and low-frequency content can result. The cause is usually power supply return currents from the motherboard that partially flow through the computer chassis to the power supply housing rather than entirely through the power supply cabling.

Follow these guidelines to mitigate the ground loop noise for PXI devices:

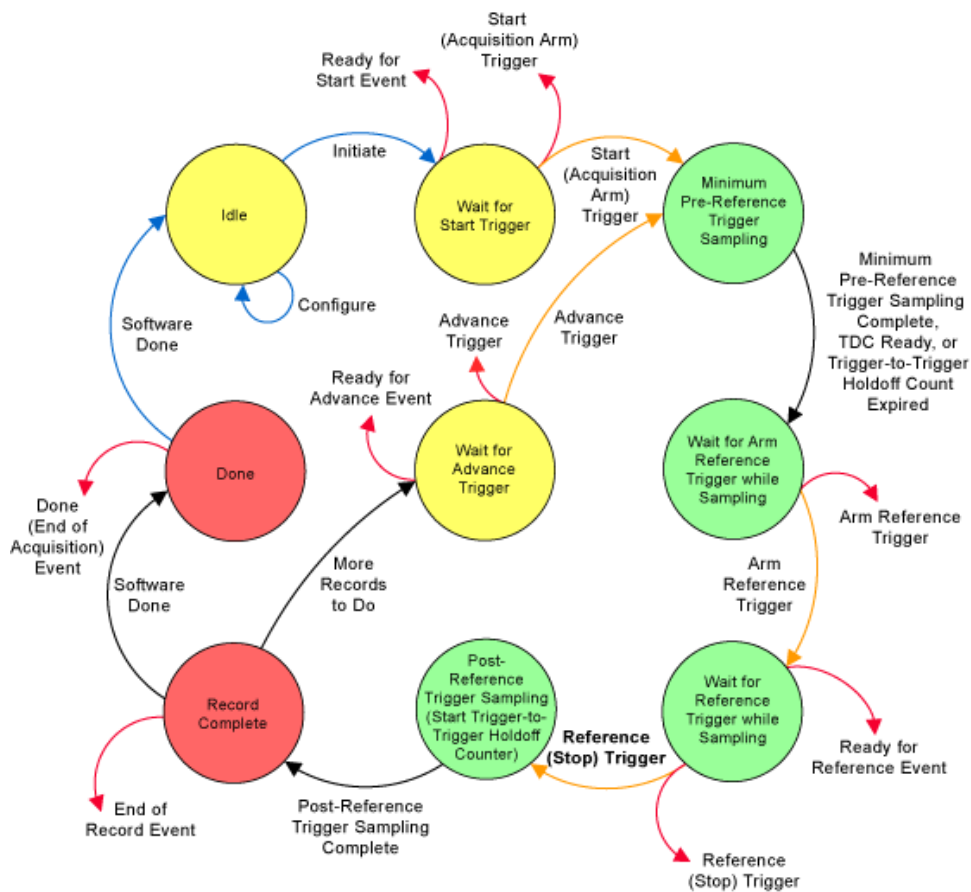
1. Ensure that the screws on the front panel of the device are tightened down.
2. Ensure that any external equipment that is providing a signal, and is not floating with respect to ground (for example, it is not a passive sensor or a battery-operated device), is connected to the same ground as the chassis.
3. Ensure all SMA cables are properly seated and that cable construction or shielding is not compromised.
4. On rack mounted systems, ground the chassis to the metal rack mount to reduce ground loop currents.

SMC-Based Oscilloscopes Acquisition Engine State Diagram



Note This functionality is only available when using NI-SCOPE.

The following figure shows the acquisition engine state diagram for SMC-Based oscilloscopes.



Note The **Reference (Stop) Trigger** is the same as the trigger level input of any traditional benchtop oscilloscope. To configure the device to behave as a traditional benchtop oscilloscope, configure only this trigger using the **niScope Configure Trigger** function.

Arrow Color	Indication
Blue	State transitions always caused by software
Black	State transitions caused by the internal state machine of the device
Red	Output signals
Orange	User-configurable state transitions caused by software or hardware

NI SMC-based oscilloscopes can be in any of the following basic states during the course of operation.

Idle—The module is not sampling a waveform. All the session attributes can be

programmed in this state. In this state, the attributes have not necessarily been applied to hardware yet, so the hardware configuration of the module may not match the session attribute values. Also, the module remains configured as it was the last time a session was committed. When `initiate` is called on the module, all the attributes are programmed to the hardware. If the computer has just been reset, or `niScope_ResetDevice` has just been called, the module is in the Idle state.

Wait for Start Trigger—On initiating an acquisition, the module transitions to this state. If the Start (Acquisition Arm) Trigger Source is configured to Immediate, the module immediately transitions out of this state and generates a Start Trigger Event. If the Start Trigger Source has been configured for software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, it transitions out of this state on the next clock cycle and generates a Start Trigger Event. The default Start Trigger Source is Immediate.

Minimum Pre-Reference Trigger Sampling—The module can transition into this state two ways: receiving the Start (Acquisition Arm) Trigger from the Start (Acquisition Arm) Trigger Source or receiving the Advance Trigger from the Advance Trigger Source. Transitioning into this state depends on the previous state of the module. While in this state, the module samples according to the session attributes configured. The module remains in this state until three conditions are satisfied: the minimum Pre-Reference Trigger sampling completes, the TDC is ready, and the trigger-to-trigger holdoff count has expired. The minimum Pre-Reference Trigger sampling is at least the user-configured Minimum Record Length multiplied by the user-configured Reference Position. The first time through this state, the trigger-to-trigger holdoff does not have an effect. When the three conditions have been satisfied, the module transitions out of this state on the next clock cycle.

Wait for Arm Reference Trigger while Sampling—After the module finishes the Minimum Pre-Reference Trigger Sampling state, the module transitions into this state. While in this state, the module continues to acquire Pre-Reference Trigger samples according to the session attributes configured. If the Arm Reference Trigger Source is configured to Immediate, the module transitions out of this state on the next clock edge. If the Arm Reference Trigger Source has been configured for a software trigger or a hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, the module transitions out of this state. The default Arm Reference Trigger Source is

Immediate.

Wait for Reference Trigger while Sampling—After the module receives Arm Reference Trigger from the Arm Reference Trigger Source, the module transitions into this state. If the Reference Trigger Source has been configured for a software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. When the module recognizes a trigger condition, the module transitions out of this state. The default Reference Trigger Source is Immediate.

Post-Reference Trigger Sampling—After the module receives the Reference (Stop) Trigger, the module transitions into this state. At the beginning of this state, the module starts a trigger-to-trigger holdoff counter. This holdoff counter corresponds to the user-configurable **Trigger Holdoff** attribute and is used in the Minimum Pre-Reference Trigger Sampling State. You can use the **Trigger Holdoff** attribute to delay the module from looking for a Reference Trigger between records. At the same time, the trigger-to-trigger holdoff counter is started, the module begins sampling Post-Reference Trigger samples according to the session attributes configured. When the Post-Reference Trigger sampling is completed, the module transitions out of this state.

Record Complete—After the module completes Post-Reference Trigger sampling, the module transitions into this state. The module leaves this state after the current record has been stored in the onboard memory. Upon leaving this state, the module outputs an End of Record Event.

Wait for Advance Trigger—After the module has completed a record and determines that there are still more records to complete, the module transitions into this state. If the Advance Trigger Source is configured to immediate, the module transitions out of this state on the next clock edge. If the Advance Trigger Source has been configured for software or hardware trigger from one of the available sources, the module remains in this state until the configured trigger occurs. Upon the module recognizing a trigger condition, the module transitions out of this state. The default Advance Trigger Source is Immediate.

Done—After the module completes a record and determines that all the records are done, it transitions into this state. Upon entering this state, the module outputs the End of Acquisition Event, which is a temporary state. The software transitions the module out of this state and back to the Idle state when you call either Fetch or Check Status.

Related information:

- [Triggering](#)
- [Trigger Types](#)
- [NI-SCOPE LabVIEW VIs](#)
- [How To Use Start Trigger Function with NI-SCOPE](#)

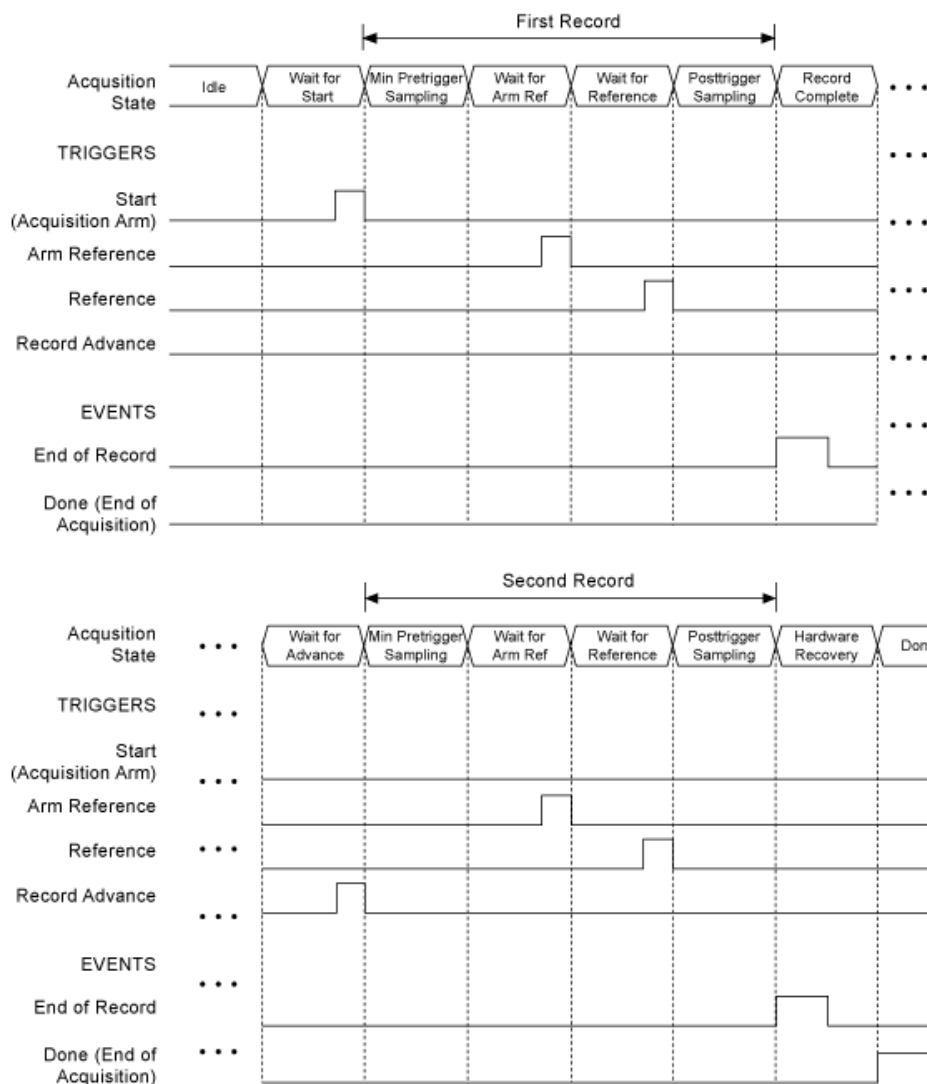
SMC-Based Oscilloscopes Timing Diagram



Note This functionality is only available when using NI-SCOPE.

SMC-Based oscilloscopes support multirecord acquisitions, which allow the capture of multiple triggered waveforms without software intervention. In this mode, the device automatically begins storing a new record to onboard memory a short time after finishing the previous record. The number of records and record size are both configurable.

The following timing diagram illustrates how the PXIe-5170/5171 reacts to the user-configurable input triggers during a multirecord acquisition.



Each state prefixed by Wait for is a state in which an input trigger can be configured. This trigger tells the device when to transition out of that particular state. The hardware is only sensitive to a particular trigger when in that trigger's appropriate Wait for state. For example, the hardware is not sensitive to a high level on the Advance Trigger until it enters the Wait for the Advance trigger state.



Note The trigger signals in the timing diagram assume active high level triggers.

The exportable events are also shown in the timing diagram. The End of Record Event is generated once per record when the device has acquired all of its pre- and post-Reference Trigger samples. This signal can be used for handshaking between devices in a system. The Done Event asserts when all of the records have been completed, but

it does not assert if the acquisition is aborted or times out.

PXIe-5170/5171 Routing Matrix



Note This functionality is only available when using NI-SCOPE.

The following table shows the signals available for export from the PXIe-5170/5171 and the lines to which they can be routed.

Source	Destination		
	PXI_Trig <0..6>	CLK OUT	PFI <0..1>
Exported Clocks			
Reference Clock	—	√	—
Sample Clock	—	—	—
Triggers			
Acquisition Arm (Start) Trigger	√	—	√
Reference (Stop) Trigger	√	—	√
Events			
End of Record Event	√	—	√
End of Acquisition Event	√	—	√
Ready for Start Event	√	—	√
Ready for Reference Event	√	—	√
Ready for Advance Event	√	—	√

For more information about the routing capabilities of the PXIe-5170/5171, refer to the PXIe-5170/5171 Block Diagram and SMC-Based Oscilloscopes Timing Diagram.

Related concepts:

- [Block Diagram](#)
- [SMC-Based Oscilloscopes Timing Diagram](#)

PXIe-5170/5171 Analog Trigger Types



Note By default, this functionality is only available when using NI-SCOPE.

The PXIe-5170/5171 supports analog edge, hysteresis, and window trigger types.

Related information:

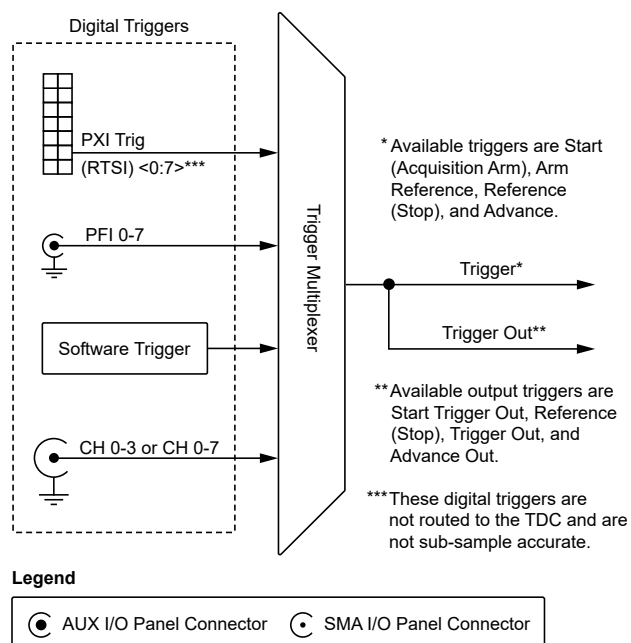
- [Edge Triggers](#)
- [Hysteresis Triggers](#)
- [Window Triggers](#)

PXIe-5170/5171 Trigger Sources



Note By default, this functionality is only available when using NI-SCOPE.

The following figure shows the trigger sources for PXIe-5170/5171 oscilloscopes.



PXle-5170/5171 Analog Trigger Paths

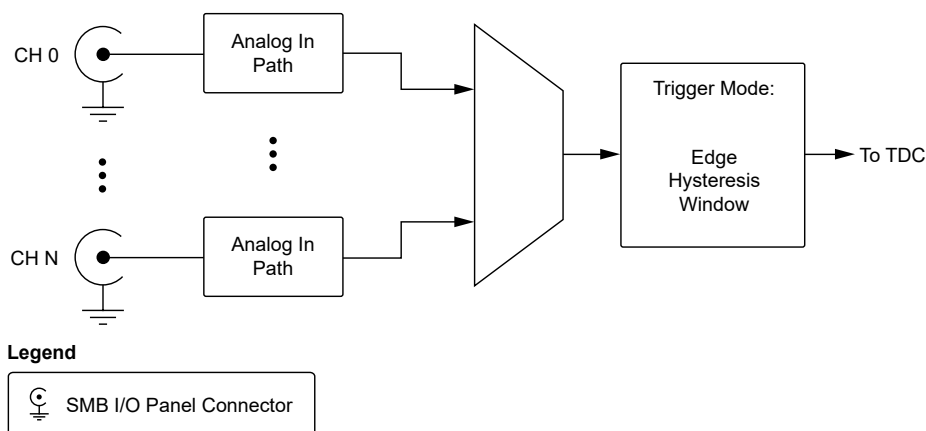
The PXle-5170/5171 provides flexible, high-precision, low-jitter triggering features.

Trigger Channels

You can use a disabled analog input channel as a trigger. For instructions on using a disabled channel to trigger acquisitions, refer to the NI KnowledgeBase.

Analog Trigger Paths

The PXle-5170/5171 uses the interpolated, predecimated digitized data from the input channel ADC when performing an analog trigger on any of the channels. This behavior ensures sub-sample level and time trigger accuracy. The following figure shows the analog trigger paths for the PXle-5170/5171. Channel count has been abstracted.



PXle-5170/5171 Trigger Holdoff



Note By default, this functionality is only available when using NI-SCOPE.

For the PXle-5170/5171, the holdoff timer is started by the Reference Trigger. When the current record finishes and the minimum number of pretrigger samples for the next record have been acquired, the holdoff timer is evaluated. If the timer has expired, the device arms its Reference Trigger circuit. If the timer has not expired, the device continues pretrigger sampling until the timer expires, and then arms its Reference Trigger circuit. Holdoff is applied for each Reference Trigger during a multirecord

acquisition. It is meaningless to apply a trigger holdoff on a single-record or continuous acquisition.

For practical purposes, the maximum trigger holdoff time is unlimited.

PXle-5170/5171 Trigger Delay



Note By default, this functionality is only available when using NI-SCOPE.

Trigger delay, which is specified in seconds, is achieved by physically delaying the output of the trigger block by a multiple of the 125 MHz Data Clock. NI-SCOPE then offsets the trigger time by an amount of time less than one period of the Data Clock in order to achieve more delay precision than the 125 MHz Data Clock allows on its own.

The maximum trigger delay is 18,014,398 seconds (approximately 6.8 months).

PXle-5170/5171 FPGA

The PXle-5170/5171 allows access to the onboard FPGA using LabVIEW FPGA Module, allowing you to directly alter the behavior of the device. This section outlines the digital capabilities of the FPGA and the methods for interfacing between FPGA resources and your application.

Xilinx Kintex-7 FPGA

The PXle-5170 contains a Xilinx Kintex-7 XC7K325T FPGA, and the PXle-5171 contains a Xilinx Kintex-7 XC7K410T FPGA.

The FPGA is used for HOST interaction over the PCI Express interface, system configuration, digital data movement, and digital signal processing. The FPGA has direct connections to:

- device ADCs
- the PCI Express bus (through DMA FIFOs, Controls, and Indicators)
- DRAM
- PFI

- Synchronization resources
- PXI trigger lines

These connections allow for custom programming using LabVIEW FPGA Module to meet the needs of many types of applications.

Reconfigurable FPGA Resources

The FPGAs in the PXIe-5170/5171 have the following resources:

Resource Type	PXIe-5170	PXIe-5171
Slice registers	407,600	508,400
Slice look-up tables (LUT)	203,800	254,200
DSPs	840	1,540
18 Kb block RAMs	890	1,590

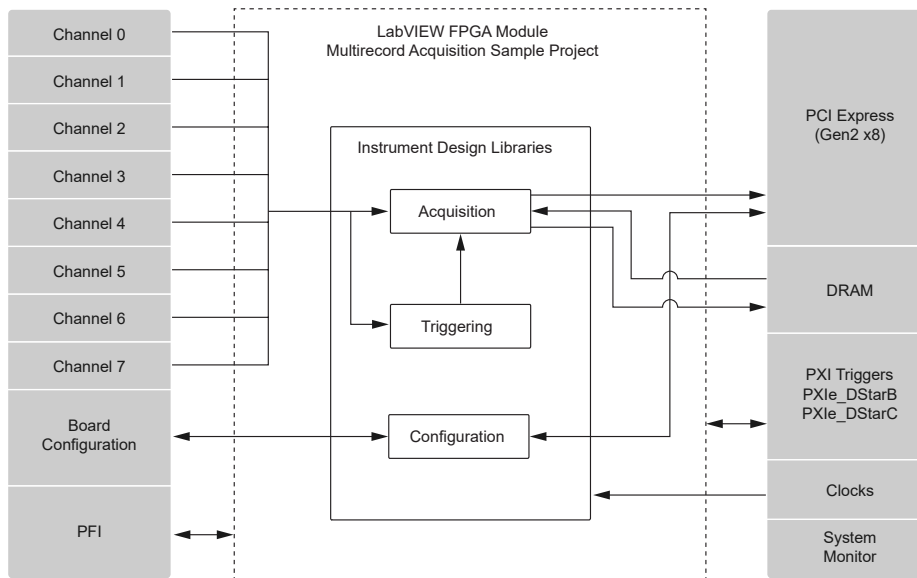
Note that some of these resources are consumed by the logic necessary to operate the device and integrate with LabVIEW FPGA Module, and are thus out of the control of users. For information on determining how many resources your design utilizes or requires, refer to the LabVIEW FPGA Module Help.

FPGA I/O Elements



Note This functionality is only available when using instrument design libraries.

Portions of the FPGA are reserved for fixed functions of your device and are not intended for customization. Other logic is provided to users as LabVIEW FPGA source and can be used as-is or edited to customize the instrument for specific applications. For example, the PXIe-5170/5171 can be partitioned, as illustrated below, when you use the Simple Acquisition (Multirecord) Sample Project.



Black blocks contain fixed HDL implementations developed by National Instruments and exposed through LabVIEW FPGA I/O Nodes or Methods.

Grey blocks contain modular LabVIEW FPGA IP distributed with LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries). You may use all or some of the instrument design libraries to customize your device. The instrument design libraries are most effective when you use them to build custom logic, rather than modifying the code inside the libraries themselves. You can interface with these blocks on the LabVIEW block diagram.

The white, dotted-line block contains LabVIEW FPGA code made available through LabVIEW Sample Projects. The sample projects are installed with LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes. Sample projects give you a ready-to-run application built using instrument design libraries, and are a good starting point for customizing your device behavior. You can also add third party IP, HDL, or other custom logic to further customize your device.

These blocks interface with each other using LabVIEW FPGA I/O elements, such as I/O Nodes and I/O Methods.

For more information on implementing custom logic, adding third-party IP, and using I/O Nodes and I/O Methods, refer to the LabVIEW FPGA Module Help.

Clocks



Note This functionality is only available when using instrument design libraries.

The following table lists the clocks available in the FPGA. In addition to these clocks, LabVIEW FPGA allows for derived clocks at user-defined frequencies, using these clocks as references. Not all clock sources may be used to derive clocks. For more information on how to create a derived clock, refer to the Creating FPGA-Derived Clocks topic in the LabVIEW FPGA Module Help.



Note The clocks in this table are available only when programming the FPGA target using LabVIEW FPGA and the instrument design libraries.

Name	Frequency (MHz)	Supports Derived Clocks?	Description
40 MHz Onboard Clock	40	Yes	Free-running 40 MHz oscillator.
PXle_Clk100	100	Yes	100 MHz clock from the backplane.
Data Clock	125	No	ADC Clock (Sample Clock) divided in hardware by 2, provided to the ADC interface and LabVIEW FPGA, and used by the instrument design libraries. For more information on Sample Clock sources, refer to the Clocking section.
Data Clock x2	250	No	Data clock multiplied by two. This clock is useful for running overclocked DSP. For more information on Sample Clock sources, refer to the Clocking section.
Data Clock x3	375	No	Data clock multiplied by three. This clock is useful for running overclocked DSP. For more information on Sample Clock sources, refer to the Clocking section.
PXle_DStarA	120 to 250	Yes	External backplane clock driven by the System Timing Module.

Related concepts:

- [PXIe-5170/5171 Clocking](#)

I/O Resources



Note This functionality is only available when using instrument design libraries.

Use FPGA I/O nodes to connect to the device I/O. You can configure FPGA I/O nodes for reading or writing. The FPGA I/O nodes connect to the front panel I/O, backplane I/O, and internal status signals of the module. The following tables describe LabVIEW FPGA I/O resources visible in the LabVIEW project.



Note Each resource must be used inside of its **Required Clock Domain**. For more information about clock domains in LabVIEW FPGA Module, refer to the Implementing Multiple Clock Domains topic in the LabVIEW FPGA Module Help.

Sample Data In

Name	Description	Data Type	Access Method	Required Clock Domain
Channel N	Contains raw data from the channel N ADC, where N is a channel number from 0 to the maximum channel number of your device. The data is presented as 2 samples per cycle at 125 MHz loop rate.	Array of two fixed-point numbers ¹ <±, 14, 1> ²	Read I/O Node	Data Clock
Channel Data Valid	For each channel, this array contains TRUE if the channel's sample is valid and FALSE if the channel's sample is not valid.	Array of four or eight Boolean values, depending on device	Read I/O Node	Data Clock

Name	Description	Data Type	Access Method	Required Clock Domain
		channel count		
Channel Overload	For each channel, this array contains TRUE if an overvoltage condition occurred on the channel and FALSE if no overvoltage condition occurred on the channel.	Array of four or eight Boolean values, depending on device channel count	Read I/O Node	Any

¹ The sample at index 0 corresponds to the first sample read from the ADC, while the sample at index 1 corresponds to the second sample read from the ADC. ² The $\langle \pm, 14, 1 \rangle$ notation corresponds to a signed, fixed-point number with a 14-bit word length and a 1-bit integer word length.

Time-to-Digital Converter (TDC)

Name	Description	Data Type	Access Method	Required Clock Domain
TDC Enable	Setting this value to TRUE enables the Time-to-Digital Conversion circuit (TDC). Setting this value to FALSE disables the TDC.	Boolean	Write I/O Node	Any
TDC Assert	Setting this value to TRUE asserts a digital signal (a "TDC pulse") synchronously the Data Clock signal.	Boolean	Write I/O Node	Data Clock
TDC Deassert	Setting this value to TRUE asserts a digital signal (a "TDC pulse") synchronously to the PXIe_Clk100 signal.	Boolean	Write I/O Node	PXIe_Clk100
TDC	Signal from the TDC that is an expanded pulse (500x)	Boolean	Read	Any

Name	Description	Data Type	Access Method	Required Clock Domain
Expanded Pulse	generated from the use of TDC Assert and TDC Deassert. The pulsewidth of this signal is proportional to the delay between edges of Data Clock and PXIe_Clk100.		I/O Node	

Trigger and Digital

Name	Description	Data Type	Access Method	Required Clock Domain
PFI N	Controls PFI line N, where N is a PFI line number from 0 to 7. This signal is connected with the AUX I/O front panel connector of the module. To access this digital I/O line, use an FPGA I/O node configured for reading or writing, or use the Set Output Enable and Set Output Data methods.	Boolean	Read I/O Node, Write I/O Node, I/O Method	Any

PXI

Name	Description	Data Type	Access Method	Required Clock Domain
PXI_TrigN	Controls PXI trigger line N, where N is a PXI trigger line number from 0 to 7. To access this digital I/O line, use an FPGA I/O node configured for reading or writing along with the Set Output Enable and Set Output Data methods. For proper device and PXI system functionality when using PXI triggers with the LabVIEW FPGA Module, follow the guidelines in PXI Triggers.	Boolean	Read I/O Node, Write I/O Node, I/O Method	Any
PXIe_Sync100	This signal becomes TRUE one PXIe_CLK100 cycle before each rising edge of PXI_CLK10. It can be sampled and used as an enable signal to mirror the behavior of PXI_CLK10.	Boolean	Read I/O Node	PXIe_Clk100

Name	Description	Data Type	Access Method	Required Clock Domain
PXle_DStarB	Trace length matched signal driven from the System Timing Module slot to the PXle-5170/5171.	Boolean	Read I/O Node	Any
PXle_DStarC	Trace length match signal driven from the PXle-5170/5171 to the System timing module.	Boolean	Write I/O Node	Any

Device Status

You can monitor device status, power, and temperature using instrument design libraries. For more information on device monitoring, refer to the overview of the Configuration instrument design library.

Name	Description	Data Type	Access Method	Required Clock Domain
Module Temperature	This resource provides the FPGA temperature reading from the on-chip temperature sensor. To calculate the value in degrees Celsius, use the following transfer function: $\text{Temperature (}^{\circ}\text{C)} = [(\text{Temperature Measurement} * 503.975) / 4096] - 273.15$	16-bit signed integer	Read I/O Node	40 MHz Onboard Clock
Module Power Consumption	This resource provides the current device power consumption reading. This instantaneous power reading is the sum of the power consumption reports of the 3.3 V sensor and the 12 V sensor. The reading is in centiWatts (cW). To calculate the value in Watts, use the following transfer function: $\text{Power Consumption (W)} = \text{Power Measurement} / 100$	16-bit signed integer	Read I/O Node	40 MHz Onboard Clock
Temperature Error	Returns TRUE when the module has exceeded its safe operating temperature range. If this condition occurs, shut down the chassis and check for proper cooling.	Boolean	Read I/O Node	Any
AUX I/O Power Enable	Setting this value to TRUE enables the 3.3 V power source from the AUX I/O front panel connector.	Boolean	Write I/O Node	Any

Name	Description	Data Type	Access Method	Required Clock Domain
AUX I/O Power Fault	Returns TRUE if an overcurrent condition has occurred at the 3.3 V power source from the AUX I/O front panel connector. For more information, refer to External Power.	Boolean	Read I/O Node	Any

Related concepts:

- [Clocks](#)
- [PXI Triggers](#)
- [PXIe-5170/5171 External Power](#)

I/O Methods



Note This functionality is only available when using instrument design libraries.

Name	Description	Clock Domain
Device Registers	Function used to read and write registers in the fixed portions of the design. These methods are intended for use only by the instrument design libraries. Use of this method outside of the instrument design libraries may result in aberrant behavior.	40 MHz Onboard Clock

PFI Trigger I/O Methods

Name	Description	Clock Domain
Set Output Data	Writes a boolean to the digital line without enabling the line.	Any
Set Output Enable	Determines whether the digital line reads external data or writes output. Wiring TRUE to Set Output Enable allows the digital line to write data. Wiring FALSE to Set Output Enable allows the digital line to read external data.	Any

PXI Triggers



Note This functionality is only available when using instrument design libraries.

You can use the FPGA I/O Node to access the eight PXI trigger lines, eight PFI lines, and two DSTAR differential trigger lines on the PXIe-5170/5171. The Data Trigger instrument design library contains IP that can operate on signals received on any of these trigger resources.

PXI Trigger lines are bussed across the backplane to all peripheral devices, so they must be reserved by the application to prevent double-driving the lines and potentially damaging third-party PXI Express devices.

Since the eight PXI trigger lines are bidirectional signals, their configuration must include a direction control, which is accessed through an I/O Method. Alternately, PXIe_DStar_B is a dedicated point-to-point signal driven from the System Timing Module slot while PXIe_DStar_C is a dedicated point-to-point signal driven to the System Timing Module slot.

When developing an FPGA VI that uses these trigger resources, reserve the trigger lines you are using to ensure compatibility with other NI devices. Refer to the PXI Specifications Tutorial for more information about trigger bus requirements.

Related concepts:

- [I/O Methods](#)
- [Reserving PXI Trigger Resources](#)

Related information:

- [PXI Specifications Tutorial](#)

Reserving PXI Trigger Resources



Note This functionality is only available when using instrument design

libraries.

National Instruments recommends that you reserve the trigger lines used by NI PXI Express devices. If two PXI Express devices try to drive the same trigger line in different applications or if the PXI Express devices are not programmed to work together, the application does not work and, in some cases, third-party PXI Express devices can be damaged. You can use Measurement & Automation Explorer (MAX) or the LabVIEW FPGA host VI to reserve trigger lines.

Reserving Trigger Lines in MAX

If you download and run the FPGA VI interactively, you should configure the PXI Express triggers in MAX. MAX maintains the trigger reservation for the NI device even after you cycle power to the PXI Express chassis.

Reserving Trigger Lines in the LabVIEW FPGA Host VI

If you download and run the FPGA VI programmatically, you should reserve the PXI Express triggers in the host VI. Use the Invoke Method function to reserve the trigger or release the trigger reservation. LabVIEW releases the trigger reservation for the NI device automatically when you close the FPGA VI reference. You must run the host VI again to reserve the trigger.

Complete the following steps to reserve a trigger line for an NI PXI Express device using the host VI.

1. Place the **Open FPGA VI Reference** function on the block diagram and configure it for the FPGA device and FPGA VI.
2. Place the **Invoke Method** function on the block diagram.
3. Wire the **FPGA VI Reference Out** output of the Open FPGA VI Reference function to the **FPGA VI Reference In** input of the Invoke Method function.
4. Wire the **error out** output of the FPGA VI Reference function to the **error in** input of the Invoke Method function.
5. Click the Invoke Method function and select **Reserve PXI Trigger** from the shortcut menu.
6. Right-click the **Trigger** input and select **Create»Constant**. An enum constant is created to help you select the trigger.

To reserve multiple trigger lines, repeat steps 2 to 6 for each trigger line you want to reserve, wiring the **FPGA VI Reference Out** output of the existing Invoke Method function to the **FPGA VI Reference In** input of the Invoke Method node that follows it.

Releasing Trigger Lines

Complete the following steps to release a trigger line for an NI PXI Express device.

1. Place the **Open FPGA VI Reference** function on the block diagram and configure it for the FPGA device and FPGA VI.
2. Place the **Invoke Method** function on the block diagram.
3. Wire the **FPGA VI Reference Out** output of the Open FPGA VI Reference function to the **FPGA VI Reference In** input of the Invoke Method function.
4. Wire the **error out** output of the FPGA VI Reference function to the **error in** input of the Invoke Method function.
5. Click the Invoke Method function and select **Unreserve PXI Trigger** from the shortcut menu.
6. Right-click the Trigger input and select **Create»Constant**. An enum constant is created to help you select the trigger.

To release multiple trigger lines, repeat steps 2 to 6 for each trigger line you want to release, wiring the **FPGA VI Reference Out** output of the existing Invoke Method function to the **FPGA VI Reference In** input of the Invoke Method node that follows it.

Configuring Trigger Pulses



Note This functionality is only available when using instrument design libraries.

To ensure compatibility with other NI devices, configure trigger pulses on an NI PXI Express device to last for at least two clock cycles of the clock on the receiving device. For example, if the clock on the receiving device is 8 MHz, which is a clock period of 125 nanoseconds, the trigger line must be constant for at least 250 nanoseconds, which is two cycles of an 8 MHz clock.



Note Regardless of the clock speed, pulses on the trigger line must be

constant for at least 18 nanoseconds. Refer to the PXI Specifications Tutorial for more information about trigger timing parameters.

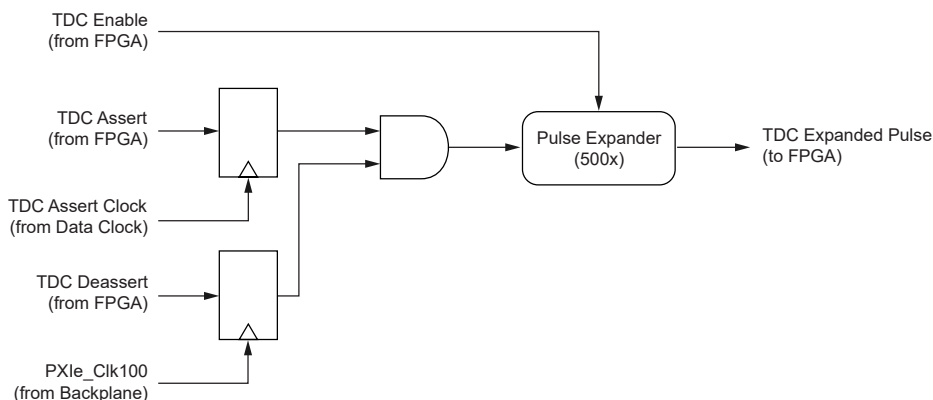
The clocks between an NI PXI Express device and another device might not be perfectly synchronized. If you assert a trigger line on a NI PXI Express device, you cannot determine at what point in the clock period the trigger registers in the receiving flip-flop. If the trigger arrives during the setup or hold time of the receiving flip-flop, you cannot determine the state of the line for that clock period. Asserting the trigger pulse for two clock cycles ensures that at least one clock cycle on the receiving flip-flop registers as a rising edge and transfers as a trigger.

Related information:

- [PXI Specifications Tutorial](#)

Time-to-Digital Converter

The PXIe-5170/5171 has a Time-to-Digital Converter (TDC) subsystem that allows the device to measure time between an event asserted in the Sample Clock domain and an event asserted on the PXIe_Clk100 domain. This measurement may be useful for evaluating the relative timing between synchronous events and is a useful component for multi-board synchronization. A functional illustration of the TDC is shown below.



(Instrument Design Libraries) To access TDC signals, use I/O Nodes.

Related concepts:

- [PXle-5170/5171 Clocking](#)
- [I/O Resources](#)

PXle-5170/5171 DRAM



Note This functionality is only available when using instrument design libraries.

The PXle-5170/5171 has two banks of dynamic random-access memory (DRAM), which are independently accessible from the FPGA. Refer to the device specifications for information about the DRAM size and throughput. These DRAM banks are general-purpose, but they are often used for storing acquired waveforms.

Related information:

- [PXle-5170 Specifications](#)
- [PXle-5171 Specifications](#)

Configuring DRAM with FPGA Memory Items



Note This functionality is only available when using instrument design libraries.

Use the FPGA memory item interface to use DRAM in the same way that you use block memory and look-up tables (LUT). DRAM memory items appear in the **Project Explorer** window under the FPGA target. The FPGA memory item interface allows you to partition the physical DRAM banks into multiple memory items.

Complete the following steps to configure DRAM with FPGA memory items.

1. To create a target-scoped memory item, right-click the FPGA target in the **Project Explorer** window and select **New»Memory** from the shortcut menu. The **Memory Properties** dialog box appears.
2. Configure the memory item in the **Memory Properties** dialog box. Click **OK**. The memory item is now populated in the **Project Explorer** window under the target.
3. Use the memory item in an FPGA VI.

PXIe-5170/5171 External Power



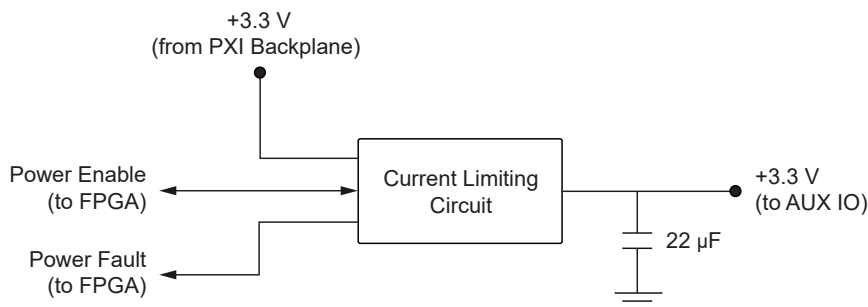
Note This functionality is only available when using instrument design libraries.

The PXIe-5170/5171 is capable of providing 3.3 V of power (200 mA nominal) to external devices through the AUX I/O connector. Power drawn from this resource is limited by a current-limiting controller. If a short or partial short occurs during operation while external power is enabled, current sensors will disable the output momentarily. After 300 ms (nominal), the power will be reconnected and checked for an overcurrent condition again. This cycle occurs every 300 ms (nominal) until the fault is cleared.



Note Behavior of this circuit is affected by component temperature. Actual protection limits may change with device and ambient temperature.

By default, power is disabled. To enable and monitor external power, use the **Device Status** I/O resources. For more information about these I/O resources, refer to I/O Resources.



For the maximum current of the device, refer to the device specifications.

Related concepts:

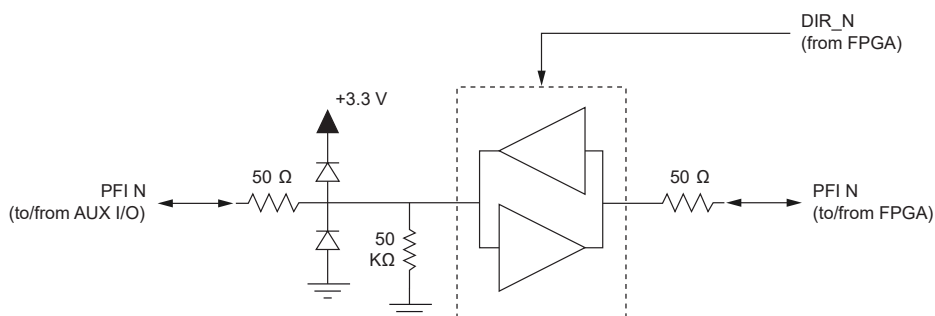
- [I/O Resources](#)

PFI

The PXle-5170/5171 includes eight general purpose digital lines. You can connect to these resources through the front panel AUX I/O port using a supported cable and accessory, such as the SCB-19 (NI part number 156053A-01). These signals are 3.3 V LVCMOS bidirectional digital signals and may be used in a variety of applications. Direction is controlled independently for each channel through the LabVIEW FPGA Module diagram.

The PFI signals are connected to the FPGA through 3.3 V LVCMOS buffers. These buffers allow for direction control, isolation to protect the FPGA from overvoltage conditions, and excellent signal quality through the matched 50 Ω output impedance. For exact I/O levels and input and output impedances, refer to the device specifications.

The digital lines are protected against overvoltage conditions. The device provides this protection through a combination of diode clamps to the +3.3 V and GND lines and a positive temperature coefficient resistor for impedance matching.

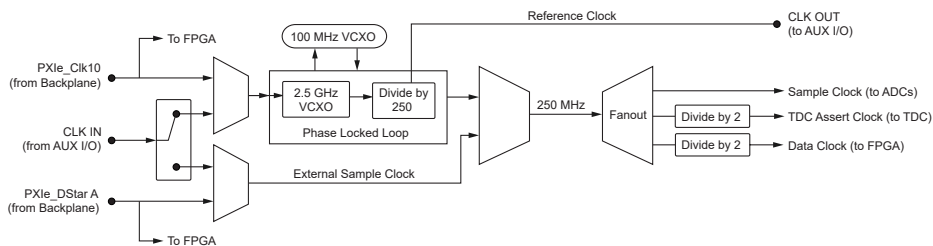


Note The interface from the PFI LVCMOS buffer to and from the FPGA is bidirectional. To guarantee that this line is not double-driven by both the FPGA and the buffer at the same time, the FPGA implements a direction control latency. This latency is an explicit delay between enabling the FPGA I/O buffer and setting the direction of the PFI. For more information on direction control latency, refer to the device specifications.

PXle-5170/5171 Clocking

The PXle-5170/5171 has flexible clocking circuitry, which allows you to generate a

250 MHz clock locked to an internal or external Reference Clock or route an external clock as a source. The main clock sourced from this circuitry is the Sample Clock, which is used to clock the ADCs and the related FPGA and synchronization logic. To configure device clocks from the host, use the Configuration instrument design library.



Sample Clock

The Sample Clock may either be generated from a 250 MHz phase-lock loop (PLL) locked to a user-selectable Reference Clock or from a user-provided external clock source connected to the AUX I/O CLK IN connector or to the PXIe_DStarA backplane signal. In the FPGA, the Data Clock is a clock source which is derived from the Sample Clock. The Data Clock runs at half the frequency of the Sample Clock. Because of this, two ADC samples per channel are provided to the FPGA for each cycle of the Data Clock.

This clock is routed to the ADCs, the FPGA, and the Time-to-Digital Conversion (TDC) circuits.



Note When using an external Sample Clock, the performance of the instrument will be dependent on the quality of that clock source. For the requirements of the CLK IN terminal, refer to the device specifications.

Reference Clock

The Sample Clock may be phase locked to different reference sources. You may lock the PLL to an internal reference, to the PXIe_Clk10 signal from the backplane, or to an external reference that you provide on the AUX I/O CLK IN pin.



Note When using an external Reference Clock, the performance of the

instrument will be dependent on the quality of that clock source. For the requirements of the CLK IN terminal, refer to the device specifications.

Exported Clock

You can use the PXIe-5170/5171 AUX I/O front panel connector to export the Reference Clock through the CLK OUT terminal. This signal will be exported using a 3.3 V LVCMOS buffer.

SMC-Based Oscilloscopes Multiple-Record Acquisition



Note This functionality is only available when using NI-SCOPE.

SMC-based oscilloscopes support multiple-record acquisition, which allows the capture of multiple triggered waveforms without software intervention. In this mode, the oscilloscope automatically begins a new acquisition in a new memory record soon after finishing the previous record. Multiple-record acquisitions can quickly acquire numerous triggered waveforms because they allow hardware rearming of the oscilloscope. Between each record, there is a dead time during which no triggers are accepted. During this time, the device sets up for the next record, as it transitions through the subsequent states of the SMC-Based Oscilloscopes Acquisition Engine State Diagram. There is also a holdoff between the last trigger in a record and the trigger of a new record. This means that the minimum time between triggers is the greater of either:

- The between-record dead time plus the time per record, or
- The user-specified holdoff time (by default, the holdoff time = 0 s).

To increase the minimum time between triggers, use the trigger holdoff feature. For more information, refer to the SMC-Based Oscilloscopes Acquisition Engine State Diagram.

Some oscilloscopes specify a minimum rearm time. Minimum rearm time is the minimum time between reference triggers as the record length approaches a minimum (for example, record length = 1 sample).

The number of records that can be acquired varies depending on the memory option of the device. Depending on the device, NI-SCOPE limits to approximately 100,000 records that can be configured without fetching during the acquisition. However, if an application allows for fetching records while they are being acquired, NI-SCOPE allows more records to be configured. Refer to [Acquiring More Records Than Fit in Digitizer Memory](#) for more information.

Related concepts:

- [SMC-Based Oscilloscopes Acquisition Engine State Diagram](#)

Related information:

- [Acquiring More Records Than Fit in Digitizer Memory](#)
- [Features Supported by NI-SCOPE Instruments](#)
- [Making Multiple-Record Acquisitions](#)

PXIe-5170/5171 Onboard Memory

The PXIe-5170/5171 allocates at least 384 bytes of onboard memory for each record in a single multirecord acquisition. Samples are stored in this buffer before transfer to the host computer. Thus the minimum size for a buffer in the onboard memory is four 96-bit samples. Software allows you to specify buffers of less than these minimum buffer sizes but only the specified number of points are transferred from onboard memory into the host computer memory.

The total number of samples that can be stored depends on the acquisition memory size option. The maximum number of records in a single multirecord acquisition is equal to the size of the memory option divided by 192 samples. Refer to the hardware specifications document for information about the memory options available for each device.

Triggering and Memory Usage

During an acquisition, samples are stored in a circular buffer that is continually rewritten until a trigger is received. These samples are known as the "pre-reference trigger" samples. After the trigger is received, the PXIe-5170/5171 continues to acquire

post-reference trigger samples. The relationship of the number of pre-reference trigger samples to post-reference trigger samples is specified by the "Reference position" attribute (by default, 50% of the record length is post-trigger.) The acquired samples are placed into onboard memory. The number of pre-reference trigger or post-reference trigger samples is only limited by the amount of onboard memory.

SMC-Based Device Synchronization



Note This functionality is only available when using NI-SCOPE.

SMC-based oscilloscopes are built on the NI Synchronization and Memory Core (SMC) technology and therefore support TCLK synchronization. Refer to the NI-TCLK Synchronization Help for more information.

Related Topics

Features Supported by SMC-Based Devices and USB Devices

Related information:

- [National Instruments Synchronization and Memory Core](#)
- [Features Supported by NI-SCOPE Instruments](#)

PXIe-5170/5171 Calibration

The PXIe-5170/5171 supports external adjustment of the following parameters:

- DC gain and offset of all DC-coupled paths
- DC offset of all AC-coupled paths
- Sample Clock frequency

Refer to the NI PXIe-5170R Calibration Procedure and NI PXIe-5171R Calibration Procedure available at ni.com/manuals for more information about calibrating the preceding parameters or information about calibrating additional specifications.

Related Topics

Summary of Calibration Options

Related concepts:

- [Summary of Calibration Options](#)

Summary of Calibration Options

The following table summarizes the available calibration options. For more information on a specific option, follow the links in the table.

Calibration	Impact	When to Use	Notes
External calibration	Calibrates DC gain, DC offset, and Sample Clock frequency	Every two years	Calibrates and verifies certain specifications
Self-calibration	Calibrates intermodule synchronization circuitry	90 days, or when temperature changes by $>5^{\circ}\text{C}$	Ensures intermodule synchronization accuracy
No calibration	No impact within 2-year calibration cycle or if temperature stays within $\pm 5^{\circ}\text{C}$	High accuracy not required outside of 5°C	—

Related concepts:

- [External Calibration](#)
- [Self-Calibration](#)

Self-Calibration

To maintain intermodule synchronization accuracy, your device provides a highly repeatable self-calibration function.

For the PXIe-5170/5171, self-calibration yields the following benefits:

- Characterizes onboard Sample Clock phase adjustment circuitry.

- Characterizes onboard intermodule synchronization measurement circuitry.
- Takes approximately 15 seconds to complete.

When to Self-Calibrate

For optimum performance, use self-calibration in the following circumstances:

- When the device is placed in a new system and has warmed up for at least 15 minutes. Warm-up begins after the chassis is powered, the device is recognized by the host, and the ADC clock is configured using the instrument design libraries. Running an included sample project or running self-calibration using NI MAX will configure the device and start warm-up.
- Any time the temperature changes more than 5 °C from the previous self-calibration
- 90 days after the previous self-calibration

The result is a product that yields full performance over its operating temperature range and two-year calibration cycle. When the two-year calibration interval expires, an external calibration is required to ensure performance that is within specification over the next two years.

The PXle-5170/5171 has a temperature sensor that monitors temperature variations. The device also records the previous self-calibration time and date. For instructions on reading the time and temperature at which self-calibration was last performed, refer to Calibration Reporting.

Running Self-Calibration

To programmatically self-calibrate the NI 5170R/5171R when using instrument design libraries, use the Self Calibrate VI located on the **Functions»FPGA Interface»Software-Designed Instruments»Oscilloscopes»NI PXle-5170R/5171R»Calibration** palette.

To programmatically self-calibrate the PXle-5170/5171 when using NI-SCOPE, use the Self Calibrate VI located on the **Functions»Measurement I/O»NI-SCOPE»Calibration** palette.

You can also self-calibrate the PXle-5170/5171 by pressing the **Self Calibrate** button for the device in MAX.

Input Connections During Self-Calibration

No special care needs to be taken on any front panel terminals during self-calibration.

Related concepts:

- [External Calibration](#)
- [Calibration Reporting](#)

External Calibration

External calibration involves both verification and adjustment. Verification is the process of testing the device to ensure that the input accuracy is within certain specifications. You can use verification to ensure that the adjustment process was successful. If verification is not successful, perform the adjustment procedure and retry the verification procedure. After a successful verification, update the calibration date using MAX or the Set Verification Date and Time VI.

Adjustment is the process of measuring and compensating for device performance to improve the input accuracy. The device is warranted to meet or exceed its published specifications for the duration of the calibration interval.

National Instruments recommends a calibration interval of two years for the PXle-5170/5171. Your application may have different calibration interval requirements based on its measurement accuracy demands. You can change the calibration due date with MAX or the Set Calibration Due Date VI.

For the PXle-5170/5171, external calibration yields the following benefits:

- Corrects for DC gain and offset errors within the oscilloscope by comparison to a precision, high-stability external voltage reference. This is done for all ranges and all filter paths (enabled/disabled).
- Corrects for DC offset errors within the oscilloscope for the AC coupling paths.
- Calibrates internal Sample Clock frequency to ensure accurate sample rate by comparison to a precision, high-stability external reference frequency.

Your device must be externally calibrated at least once every two years in order to maintain adherence to published specifications.

Calibration procedures may be found online at ni.com/manuals.

You can learn more about external calibration at ni.com/calibration.

Related information:

- [Calibration](#)

Calibration Reporting

Reports may be obtained from your device regarding time and temperature at which calibrations were run on your device. To view this information, use the VIs located on the **Functions»Software-Designed Instruments»Oscilloscopes»NI PXIe-5170R/5171R»Calibration»Utilities** palette.

You can also view this information in MAX and through the NI System Configuration API.

For more information about these VIs and the calibration instrument design libraries, refer to the Calibration Data and Calibration API overview pages.

PXIe-5170/5171 Warm-Up

NI recommends warming up the PXIe-5170/5171 for 15 minutes before operation. The unit is fully functional prior to this time, but frequency and amplitude accuracy and other specifications are not guaranteed until the device has fully completed warming up.



Note Warm-up begins after the chassis is powered, the device is recognized by the host, and the device is configured using the instrument design libraries or NI-SCOPE. Running an included sample project or running self-calibration using MAX will configure the device and start warm-up.

PXIe-5170/5171 Power On, Reset, and Download Conditions

The PXIe-5170/5171 applies certain conditions to the device state at power on, device reset, and download. The PXIe-5170/5171 also applies certain conditions to the device state upon FPGA reset.

Power On and Download Conditions

The following conditions apply to the device state after powering on the device, restarting the device, or downloading a new FPGA VI to the device.

- PFI lines are configured as input terminals.
- Signal conditioning peak-to-peak range (V_{pk-pk}) is set to 5 V, coupling is disabled, and filter is set to 100 MHz.
- PXI trigger lines are configured as input terminals.
- Clocking is reset to the component default state.
- External power is enabled and connected directly to the FPGA Window.
- ADCs are reset to the component default state.

Reset Conditions

The following conditions apply to the device state after resetting the device FPGA.

- PFI lines are configured as input terminals.
- Signal conditioning range is maintained.
- PXI trigger lines are configured as input terminals.
- Clock states are maintained.
- External power state is maintained.
- ADC states are maintained.